

# ZED-F9T-10B

## High accuracy timing module Professional grade

Data sheet



#### Abstract

This data sheet describes the ZED-F9T timing module with multi-band GNSS receiver and nanosecond-level timing accuracy. ZED-F9T meets the most stringent 5G timing requirements, is ideal for global deployment due to GPS, BeiDou, Galileo, and GLONASS reception, and is unaffected by ionospheric errors. The module provides differential timing mode for highly accurate local timing and built-in security for highest robustness against malicious attacks.

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UBX-20033635 - R09 C1-Public



## **Document information**

Title	ZED-F9T-10B	
Subtitle	High accuracy timing module	
Document type	Data sheet	
Document number	UBX-20033635	
Revision and date R09 25-Apr-202		25-Apr-2024
Disclosure restriction	C1-Public	

Product status	Corresponding content status	
Functional Sample	Draft	For functional testing. Revised and supplementary data will be published later.
In development / prototype	Objective specification	Target values. Revised and supplementary data will be published later.
Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

#### This document applies to the following products:

Product name	Type number	FW version	IN/PCN reference	Product status
ZED-F9T	ZED-F9T-10B-01	TIM 2.20	UBX-21050800	Mass production

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## **1** Functional description

### 1.1 Overview

The ZED-F9T-10B is a multi-band GNSS module offering 5 ns (1-sigma) timing accuracy with unparalleled low power consumption.

The ZED-F9T-10B incorporates the u-blox F9 multi-band platform in a small surface-mount device with a form factor of 22 x 17 mm.

### **1.2 Performance**

Specification			
Multi-band GNSS receiver for timing applications			
Absolute timing mode	5 ns		
Differential timing mode <sup>2</sup>	2.5 ns		
	0.25 Hz to 25 MHz (configurable)		
	±4 ns		
	8 ns		
Dynamics	≤ 4 g		
Altitude	80,000 m		
Velocity	500 m/s		
	0.05 m/s		
	0.3 deg		
	Multi-band GNSS receiver for tim Absolute timing mode Differential timing mode <sup>2</sup> Dynamics Altitude	Multi-band GNSS receiver for timing applications         Absolute timing mode       5 ns         Differential timing mode <sup>2</sup> 2.5 ns         0.25 Hz to 25 MHz (configurable)         ±4 ns         8 ns         Dynamics       ≤ 4 g         Altitude       80,000 m         Velocity       500 m/s         0.05 m/s	

Table 1: ZED-F9T-10B specifications

GNSS		GPS+GLO+GAL+BDS	GPS+BDS+GAL	GPS+GAL	GPS+GLO	GPS+BDS	GPS
Acquisition <sup>5</sup>	Cold start	24 s	25 s	29 s	26 s	28 s	29 s
	Hot start	2 s	2 s	2 s	2 s	2 s	2 s
	Aided start <sup>6</sup>	2 s	2 s	2 s	2 s	2 s	2 s
Max navigation update rate <sup>7</sup>		8 Hz	10 Hz	15 Hz	15 Hz	12 Hz	20 Hz

Table 2: ZED-F9T-10B performance in different GNSS modes

<sup>3</sup> Assuming Airborne 4 g platform

<sup>&</sup>lt;sup>1</sup> 1-sigma, fixed position mode, depends on temperature, atmospheric conditions, baseline length, GNSS antenna, multipath conditions, satellite visibility and geometry

<sup>&</sup>lt;sup>2</sup> Demonstrated with 20 km baseline

<sup>4 50%</sup> at 30 m/s for dynamic operation

<sup>&</sup>lt;sup>5</sup> Commanded starts. All satellites at -130 dBm. Measured at room temperature. Dual band operation

<sup>&</sup>lt;sup>6</sup> Dependent on the speed and latency of the aiding data connection, commanded starts

<sup>&</sup>lt;sup>7</sup> 95% In PVT navigation mode, assumes secondary navigation output disabled (default)



GNSS	GPS+GLO+GAL+BDS	GPS+BDS+GAL	GPS+GAL	GPS+GLO	GPS+BDS	GPS
Horizontal position accuracy (CEP)	1.5 m	1.5 m	1.5 m	1.5 m	1.5 m	1.5 m

Table 3: ZED-F9T-10B position accuracy in different GNSS modes

In order to achieve the best absolute timing accuracy, measure the propagation delay of the entire signal path from the antenna to the receiver's time pulse output, and then compensate for this delay using the CFG-TP configuration items.

GNSS		GPS+GLO+GAL+BDS
Sensitivity <sup>9</sup>	Tracking and nav.	-167 dBm
2	Reacquisition	-160 dBm
	Cold start	-148 dBm
	Hot start	-157 dBm

Table 4: ZED-F9T-10B sensitivity

#### **1.3 Supported GNSS constellations**

The ZED-F9T-10B GNSS module is a concurrent GNSS receiver that can receive and track multiple GNSS systems. Thanks to the multi-band RF front-end architecture, all four major GNSS constellations (GPS, Galileo, GLONASS and BeiDou) as well as NavIC, SBAS and QZSS satellites can be received concurrently. If low power consumption is a key factor, then the receiver can be configured for a subset of GNSS constellations.

The ZED-F9T-10B can receive the NavIC L5 satellite signals that share the same frequency with GPS L5 signals and can be configured to work on its own or in parallel with the other GNSS constellations.

The QZSS system shares the same frequency bands with GPS and can only be processed in conjunction with GPS.

To benefit from multi-band signal reception, dedicated hardware preparation must be made during the design-in phase. See the Integration manual [1] for u-blox design recommendations.

The ZED-F9T-10B supports the GNSS and their signals as shown in Table 5.

GPS/QZSS	GLONASS	Galileo	BeiDou	NavIC
L1C/A (1575.420 MHz)	L1OF (1602 MHz + k*562.5 kHz, k = –7,,6)	E1-B/C (1575.420 MHz)	B1I (1561.098 MHz) B1C (1575.420 MHz) <sup>10</sup>	-
L5 (1176.450 MHz)	-	E5a (1176.450 MHz)	B2a (1176.450 MHz)	SPS-L5 (1176.450 MHz)

Table 5: Supported GNSS signals on ZED-F9T-10B

The ZED-F9T-10B can use the u-blox AssistNow<sup>™</sup> Online service which provides GNSS assistance information.

<sup>&</sup>lt;sup>8</sup> Depends on atmospheric conditions, GNSS antenna, multipath conditions, satellite visibility, and geometry

<sup>&</sup>lt;sup>9</sup> Demonstrated with a good external LNA. Measured at room temperature.

<sup>&</sup>lt;sup>10</sup> BeiDou B1I and B1C signals are not to be enabled concurrently



### 1.4 Supported GNSS augmentation systems

#### 1.4.1 Quasi-Zenith Satellite System (QZSS)

The Quasi-Zenith Satellite System (QZSS) is a regional navigation satellite system that provides positioning services for the Pacific region covering Japan and Australia. The ZED-F9T-10B is able to receive and track QZSS L1 C/A and L5 signals concurrently with GPS signals, resulting in better availability especially under challenging signal conditions, e.g. in urban canyons.

**QZSS** can be enabled only if GPS operation is also configured.

#### 1.4.2 Satellite-based augmentation system (SBAS)

The ZED-F9T-10B supports SBAS (including WAAS in the US, EGNOS in Europe, L1Sb(QZSS SBAS) in Japan and GAGAN in India) to deliver improved location accuracy within the regions covered. However, the additional inter-standard time calibration step used during SBAS reception results in degraded time accuracy overall.

SBAS reception is disabled by default in ZED-F9T-10B.

#### 1.4.3 Differential timing mode

To improve timing accuracy locally, the ZED-F9T-10B can be used in differential timing mode, in which correction data is sent to neighboring ZED-F9T-10B timing receivers via a communication network.

In differential timing mode the ZED-F9T-10B can operate either as a reference station generating the following RTCM 3.3 messages, or as a corrected station using the following RTCM 3.3 messages:

Message type	Description
RTCM 1005	Stationary RTK reference station ARP
RTCM 1077	GPS MSM7
RTCM 1087	GLONASS MSM7
RTCM 1097	Galileo MSM7
RTCM 1127	BeiDou MSM7
RTCM 1230	GLONASS code-phase biases
RTCM 4072.1	Additional reference station information (u-blox proprietary RTCM Message)

Table 6: Supported RTCM 3.3 messages

# 1.5 Broadcast navigation data and satellite signal measurements

The ZED-F9T-10B can output all the GNSS broadcast data upon reception from tracked satellites. This includes all the supported GNSS signals as well as the QZSS and SBAS augmentation services. The UBX-RXM-SFRBX message provides this information, see the Interface description [2] for the UBX-RXM-SFRBX message specification. The receiver can provide satellite signal information in a form compatible with the Radio Resource LCS Protocol (RRLP) [4].

#### 1.5.1 Carrier-phase measurements

The ZED-F9T-10B modules provide raw carrier-phase data for all supported signals, along with pseudorange, Doppler and measurement quality information. The data contained in the UBX-RXM-RAWX message follows the conventions of a multi-GNSS RINEX 3 observation file. For the UBX-RXM-RAWX message specification, see Interface description [2].





Raw measurement data are available once the receiver has established data bit synchronization and time-of-week.

### 1.6 Supported protocols

The ZED-F9T-10B supports the following protocols:

Protocol	Туре
UBX	Input/output, binary, u-blox proprietary
NMEA 4.11 (default), 4.10, 4.0, 2.3, and 2.1	Input/output, ASCII
RTCM 3.3	Input/output, binary

Table 7: Supported protocols

For specification of the protocols, see the Interface description [2].



## 2 System description

## 2.1 Block diagram



#### Figure 1: ZED-F9T-10B block diagram

An active antenna is mandatory with the ZED-F9T-10B. For more information, see the Integration manual [1].



## **3 Pin definition**

#### 3.1 Pin assignment

The pin assignment of the ZED-F9T-10B module is shown in Figure 2. The defined configuration of the PIOs is listed in Table 8.

For detailed information on pin functions and characteristics, see the Integration manual [1].

The ZED-F9T-10B is an LGA package with the I/O on the outside edge and central ground pads.



#### Figure 2: ZED-F9T-10B pin assignment

Pin no.	Name	1/0	Description
1	GND	-	Ground
2	RF_IN	I	RF input
3	GND	-	Ground
4	ANT_DETECT	I	Active antenna detect - default active high
5	ANT_OFF	0	External LNA disable - default active high
6	ANT_SHORT_N	I	Active antenna short detect - default active low
7	VCC_RF	0	Voltage for external LNA
8	Reserved	-	Reserved



Pin no.	Name	I/O	Description
9	Reserved	-	Reserved
10	Reserved	-	Reserved
11	Reserved	-	Reserved
12	GND	-	Ground
13	Reserved	-	Reserved
14	GND	-	Ground
15	Reserved	-	Reserved
16	Reserved	-	Reserved
17	Reserved	-	Reserved
18	Reserved	-	Reserved
19	GEOFENCE_STAT	0	Geofence status, user defined
20	Reserved	-	Reserved
21	Reserved	-	Reserved
22	Reserved	-	Reserved
23	Reserved	-	Reserved
24	Reserved	-	Reserved
25	Reserved	-	Reserved
26	RXD2	I	Correction UART input
27	TXD2	0	Correction UART output
28	Reserved	_	Reserved
29	Reserved	-	Reserved
30	Reserved	-	Reserved
31	Reserved	-	Reserved
32	GND	-	Ground
33	VCC	I	Voltage supply
34	VCC	I	Voltage supply
35	Reserved	-	Reserved
36	V_BCKP	I	Backup supply voltage
37	GND	-	Ground
38	V_USB	I	USB supply
39	USB_DM	I/O	USB data
40	USB_DP	I/O	USB data
41	GND	-	Ground
42	TXD/SPI_SDO	0	Host UART output if D_SEL = 1(or open). SPI_SDO if D_SEL = 0
43	RXD/SPI_SDI	I	Host UART input if D_SEL = 1(or open). SPI_SDI if D_SEL = 0
44	SDA/SPI_CS_N	I/O	I2C Data if D_SEL = 1 (or open). SPI Chip Select if D_SEL = 0
45	SCL/SPI_CLK	I/O	I2C Clock if D_SEL = 1 (or open). SPI Clock if D_SEL = 0
46	Reserved	-	Reserved
47	D_SEL	I	Interface select for pins 42-45
48	GND	-	Ground
49	RESET_N	I	RESET_N
50	SAFEBOOT_N	I	SAFEBOOT_N (for future service, updates and reconfiguration, leave OPEN)
51	EXTINT	I	External interrupt pin
52	EXTINT2	I	External interrupt pin 2





Pin no.	Name	I/O	Description
53	TIMEPULSE	0	Time pulse
54	TIMEPULSE2	0	Time pulse 2
		•	

Table 8: ZED-F9T-10B pin assignment



## **4 Electrical specifications**

### 4.1 Absolute maximum ratings

▲ CAUTION. Risk of device damage. Exceeding the absolute maximum ratings may affect the lifetime and reliability of the device or permanently damage it. Do not exceed the absolute maximum ratings.

This product is not protected against overvoltage or reversed voltages. Use appropriate protection to avoid device damage from voltage spikes exceeding the specified boundaries.

Parameter	Symbol	Condition	Min	Max	Units
Power supply voltage	VCC		-0.5	3.6	V
Voltage ramp on VCC <sup>11</sup>			20	8000	μs/V
Backup battery voltage	V_BCKP		-0.5	3.6	V
Voltage ramp on V_BCKP <sup>11</sup>			20		µs/V
Input pin voltage	Vin	VCC ≤ 3.1 V	-0.5	VCC + 0.5	V
		VCC > 3.1 V	-0.5	3.6	V
VCC_RF output current	ICC_RF			300	mA
Supply voltage USB	V_USB		-0.5	3.6	V
USB signals	USB_DM, USB_DP		-0.5	V_USB + 0.9	5 V
Input power at RF_IN	Prfin	source impedance = 50 Ω, continuous wave		10	dBm
Storage temperature	Tstg		-40	+85	°C

Table 9: Absolute maximum ratings

## 4.2 Operating conditions

Extreme operating temperatures can significantly impact the specified values. If an application operates near the min or max temperature limits, ensure the specified values are not exceeded.

Parameter	Symbol	Min	Typical	Max	Units	Condition
Power supply voltage	VCC	2.7	3.0	3.6	V	
Backup battery voltage	V_BCKP	1.65		3.6	V	
Backup battery current <sup>12, 13</sup>	I_BCKP		45		μΑ	V_BCKP = 3 V, VCC = 0 V
SW backup current <sup>13</sup>	I_SWBCKP		1.4		mA	
Input pin voltage range	Vin	0		VCC	V	
Digital IO pin low level input voltage	Vil			0.4	V	
Digital IO pin high level input voltage	Vih	0.8 * VCC			V	
Digital IO pin low level output voltage	Vol			0.4	V	lol = 2 mA
TIMEPULSE						lol = 4 mA
Digital IO pin high level output voltage	e Voh	VCC - 0.4			V	loh = 2 mA
TIMEPULSE						loh = 4 mA

<sup>&</sup>lt;sup>11</sup> Exceeding the ramp speed may permanently damage the device

<sup>&</sup>lt;sup>12</sup> To measure the I\_BCKP the receiver should first be switched on, i.e. VCC and V\_BCKP is available. Then set VCC to 0 V while the V\_BCKP remains available. Afterward measure the current consumption at the V\_BCKP.

<sup>&</sup>lt;sup>13</sup> The value has been characterized at 25 °C ambient temperature.



Parameter	Symbol	Min	Typical	Max	Units	Condition
DC current through any digital I/O pin (except supplies)	lpin			5	mA	
VCC_RF voltage	VCC_RF		VCC - 0.1		V	
VCC_RF output current	ICC_RF			50	mA	
Receiver chain noise figure <sup>14</sup>	NFtot		9.5		dB	
External gain (at RF_IN)	Ext_gain	17		50	dB	
Operating temperature	Topr	-40	+25	+85	°C	

Table 10: Operating conditions

#### 4.3 Indicative power requirements

Table 11 provides examples of typical current requirements when using a cold start command. The given values are total system supply current for a possible application including RF and baseband sections.

All values in Table 11 have been measured at 25 °C ambient temperature.

The actual power requirements vary depending on the FW version used, external circuitry, number of satellites tracked, signal strength, type and time of start, duration, and conditions of test.

Symbol	Parameter	Conditions	GPS+GLO +GAL+BDS	GPS	Unit
I <sub>PEAK</sub>	Peak current	Acquisition	130	120	mA
I <sub>VCC</sub> <sup>15</sup>	VCC current	Acquisition	90	75	mA
I <sub>VCC</sub> <sup>15</sup>	VCC current	Tracking	85	70	mA

Table 11: Currents to calculate the indicative power requirements

<sup>&</sup>lt;sup>14</sup> Only valid for GPS

<sup>&</sup>lt;sup>15</sup> Simulated GNSS signal



## **5** Communications interfaces

The ZED-F9T-10B has several communications interfaces<sup>16</sup>, including UART, SPI, I2C and USB.

All the inputs have internal pull-up resistors in normal operation and can be left open if not used. All the PIOs are supplied by VCC, therefore all the voltage levels of the PIO pins are related to VCC supply voltage.

### 5.1 UART

The UART interfaces support configurable baud rates. See the Integration manual [1].

Hardware flow control is not supported.

The UART1 is enabled if D\_SEL pin of the module is left open or "high".

Symbol	Parameter	Min	Max	Unit
R <sub>u</sub>	Baud rate	9600	921600	bit/s
$\Delta_{Tx}$	Tx baud rate accuracy	-1%	+1%	-
$\Delta_{Rx}$	Rx baud rate tolerance	-2.5%	+2.5%	-

Table 12: ZED-F9T-10B UART specifications

### 5.2 SPI

The SPI interface is disabled by default. The SPI interface shares pins with UART and I2C and can be selected by setting  $D_SEL = 0$ . The SPI interface can be operated in peripheral mode only. The maximum transfer rate using SPI is 125 kB/s and the maximum SPI clock frequency is 5.5 MHz.

The SPI timing parameters for peripheral operation are defined in Figure 3. Default SPI configuration is CPOL = 0 and CPHA = 0.



Figure 3: ZED-F9T-10B SPI specification mode 1: CPHA=0 SCK = 5.33 MHz

<sup>&</sup>lt;sup>16</sup> The signal names and related terms have been replaced with new terminology in this document.

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Symbol	Parameter	Min	Max	Unit
1	CS deassertion hold time	23	-	ns
2	Chip select time (CS to SCK)	20	-	ns
3	SCK rise/fall time	-	7	ns
4	SCK high time	24	-	ns
5	SCK low time	24	-	ns
6	Chip deselect time (SCK falling to CS)	30	-	ns
7	Chip deselect time (CS to SCK)	30	-	ns
9	CS high time	32	-	ns
10	SDI transition time	-	7	ns
11	SDI setup time	16	-	ns
12	SDI hold time	24	-	ns

Table 13: SPI peripheral input timing parameters 1 - 12

Symbol	Parameter	Min	Max	Unit
А	SDO data valid time (CS)	12	40	ns
В	SDO data valid time (SCK), weak driver mode	15	40	ns
С	SDO data hold time	100	140	ns
D	SDO rise/fall time, weak driver mode	0	5	ns
E	SDO data disable lag time	15	35	ns

Table 14: SPI peripheral timing parameters A - E, 2 pF load capacitance

000 1 1 1 1 1 (00)			
SDO data valid time (CS)	16	55	ns
SDO data valid time (SCK), weak driver mode	20	55	ns
SDO data hold time	100	150	ns
SDO rise/fall time, weak driver mode	3	20	ns
SDO data disable lag time	15	35	ns
	SDO data hold time SDO rise/fall time, weak driver mode	SDO data hold time     100       SDO rise/fall time, weak driver mode     3	SDO data hold time100150SDO rise/fall time, weak driver mode320

Table 15: SPI peripheral timing parameters A - E, 20 pF load capacitance

Parameter	Min	Max	Unit
SDO data valid time (CS)	26	85	ns
SDO data valid time (SCK), weak driver mode	30	85	ns
SDO data hold time	110	160	ns
SDO rise/fall time, weak driver mode	13	45	ns
SDO data disable lag time	15	35	ns
	SDO data valid time (CS) SDO data valid time (SCK), weak driver mode SDO data hold time SDO rise/fall time, weak driver mode	SDO data valid time (CS)26SDO data valid time (SCK), weak driver mode30SDO data hold time110SDO rise/fall time, weak driver mode13	SDO data valid time (CS)2685SDO data valid time (SCK), weak driver mode3085SDO data hold time110160SDO rise/fall time, weak driver mode1345

Table 16: SPI peripheral timing parameters A - E, 60 pF load capacitance

### 5.3 I2C

An I2C interface is available for communication with an external host CPU in I2C Fast-mode. Backwards compatibility with Standard-mode I2C bus operation is not supported. The interface can be operated only in peripheral mode with a maximum bit rate of 400 kbit/s. The interface can make use of clock stretching by holding the SCL line LOW to pause a transaction. In this case, the bit transfer rate is reduced. The maximum clock stretching time is 20 ms.





#### Figure 4: ZED-F9T-10B I2C peripheral specification

		I2C Fast-mode		
Symbol	Parameter	Min	Max	Unit
f <sub>SCL</sub>	SCL clock frequency	0	400	kHz
t <sub>HD;STA</sub>	Hold time (repeated) START condition	0.6	-	μs
t <sub>LOW</sub>	Low period of the SCL clock	1.3	-	μs
t <sub>HIGH</sub>	High period of the SCL clock	0.6	-	μs
t <sub>SU;STA</sub>	Setup time for a repeated START condition	0.6	-	μs
t <sub>HD;DAT</sub>	Data hold time	0 <sup>17</sup>	_ 18	μs
t <sub>SU;DAT</sub>	Data setup time	100 <sup>19</sup>		ns
t <sub>r</sub>	Rise time of both SDA and SCL signals	-	300 (for C = 400pF)	ns
t <sub>f</sub>	Fall time of both SDA and SCL signals	-	300 (for C = 400pF)	ns
t <sub>SU;STO</sub>	Setup time for STOP condition	0.6	-	μs
t <sub>BUF</sub>	Bus-free time between a STOP and START condition	1.3	-	μs
t <sub>VD;DAT</sub>	Data valid time	-	0.9 <sup>18</sup>	μs
t <sub>VD;ACK</sub>	Data valid acknowledge time	-	0.9 <sup>18</sup>	μs
V <sub>nL</sub>	Noise margin at the low level	0.1 VCC	-	V
V <sub>nH</sub>	Noise margin at the high level	0.2 VCC	-	V

#### Table 17: ZED-F9T-10B I2C peripheral timings and specifications

<sup>&</sup>lt;sup>17</sup> External device must provide a hold time of at least one transition time (max 300 ns) for the SDA signal (with respect to the min Vih of the SCL signal) to bridge the undefined region of the falling edge of SCL.

<sup>&</sup>lt;sup>18</sup> The maximum  $t_{HD;DAT}$  must be less than the maximum  $t_{VD;DAT}$  or  $t_{VD;ACK}$  with a maximum of 0.9 µs by a transition time. This maximum must only be met if the device does not stretch the LOW period (tLOW) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

<sup>&</sup>lt;sup>19</sup> When the I2C peripheral is stretching the clock, the  $t_{SU;DAT}$  of the first bit of the next byte is 62.5 ns.



The I2C interface is only available with the UART default mode. If the SPI interface is selected by using D\_SEL = 0, the I2C interface is not available.

### 5.4 USB

The USB 2.0 FS (full speed, 12 Mbit/s) interface can be used for host communication. Due to the hardware implementation, it may not be possible to certify the USB interface. The V\_USB pin supplies the USB interface.

Interface	Settings
UART1 output	38400 baud, 8 bits, no parity bit, 1 stop bit.
	NMEA protocol with GGA, GLL, GSA, GSV, RMC, VTG, TXT, ZDA messages are output by default
	UBX and RTCM 3.3 protocols are enabled by default but no output messages are enabled b default.
UART1 input	38400 baud, 8 bits, no parity bit, 1 stop bit.
	UBX, NMEA and RTCM 3.3 input protocols are enabled by default.
UART2 output	38400 baud, 8 bits, no parity bit, 1 stop bit.
	UBX protocol cannot be enabled.
	RTCM 3.3 protocol is enabled by default but no output messages are enabled by default.
	NMEA protocol is disabled by default.
UART2 input	38400 baud, 8 bits, no parity bit, 1 stop bit.
	UBX protocol cannot be enabled and will not receive UBX input messages.
	RTCM 3.3 protocol is enabled by default.
	NMEA protocol is disabled by default.
USB	Default messages activated as in UART1. Input/output protocols available as in UART1.
12C	Available for communication in the Fast-mode with an external host CPU in peripheral mode only. Default messages activated as in UART1. Input/output protocols available as in UART1. Maximum bit rate 400 kb/s.
SPI	Allow communication to a host CPU, operated in peripheral mode only. Default messages activated as in UART1. Input/output protocols available as in UART1. SPI is not available unless D_SEL pin is set to low (see section D_SEL interface in Integration manual [1]).

### 5.5 Default interface settings

Table 18: Default interface settings

The Refer to the applicable Interface description [2] for information about further settings.

By default, the ZED-F9T-10B outputs NMEA messages that include satellite data for all GNSS bands being received. This results in a high NMEA output load for each navigation period. Make sure the UART baud rate used is sufficient for the selected navigation rate and the number of GNSS signals being received.



#### **6** Mechanical specifications Pin 1 Indicator Μ Ρ R اللاح Z ٩ ٦ \* $\square$ $\square$ ഥ മ Ē $\square$ \* Ē G Н D L А





#### Figure 5: ZED-F9T-10B mechanical drawing

Symbol	Min (mm)	Typical (mm)	Max (mm)
A	21.80	22.00	22.20
В	16.80	17.00	17.20
С	2.20	2.40	2.60
D	3.65	3.85	4.05
E	0.85	1.05	1.25
F	1.70	1.90	2.10
G	1.05	1.10	1.15
Н	0.70	0.80	0.96
к	1.20	1.50	1.80
М	3.45	3.65	3.85
N	3.05	3.25	3.45
Р	2.05	2.10	2.15



Symbol	Min (mm)	Typical (mm)	Max (mm)
R	0.88	1.10	1.32
L	0.00		0.30
Weight		1.8 g	

#### Table 19: ZED-F9T-10B mechanical dimensions

The mechanical picture of the de-paneling residual tabs (L) is an approximate representation. The shape and position may vary.

Take the size of the de-paneling residual tabs into account when designing the component keepout area.



## 7 Qualifications and approvals

Quality and reliability	
Product qualification	Qualified according to ISO 16750
Chip qualification	Modules are based on AEC-Q100 qualified GNSS chips
Manufacturing	Manufactured at ISO/TS 16949 certified sites
Environmental	
RoHS compliance	Yes
Moisture sensitivity level (MSL) <sup>20 21</sup>	4
Type approvals	
European RED certification (CE)	Declaration of Conformity (DoC) is available on the u-blox website.
UK conformity assessment (UKCA)	Yes

Table 20: Qualifications and approvals

<sup>&</sup>lt;sup>20</sup> For the MSL standard, see IPC/JEDEC J-STD-020 and J-STD-033, available on www.jedec.org

<sup>&</sup>lt;sup>21</sup> For more information regarding moisture sensitivity levels, labelling, storage and drying, see the Product packaging reference guide [3]



## 8 Labeling and ordering information

This section provides information about product labeling and ordering. For information about product handling and soldering see the Integration manual [1].

### 8.1 Product labeling

The labeling of the ZED-F9T-10B modules provides product information and revision information. For more information, contact u-blox sales.



Figure 6: Example of ZED-F9T-10B label

### 8.2 Explanation of product codes

Three product code formats are used in the ZED-F9T-10B labels. The **Product name** used in documentation such as this data sheet identifies all u-blox products, independent of packaging and quality grade. The **Ordering code** includes options and quality, while the **Type number** includes the hardware and firmware versions.

Table 21 below details these three formats
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Format	Structure	Product code	
Product name	PPP-TGV	ZED-F9T	
Ordering code	PPP-TGV-NNQ	ZED-F9T-10B	
Type number	PPP-TGV-NNQ-XX	ZED-F9T-10B-01	

```
Table 21: Product code formats
```

The parts of the product code are explained in Table 22.

Code	Meaning	Example	
PPP	Product family	ZED	
TG	Platform	F9 = u-blox F9	
V	Variant	T = Timing	
NNQ Op	Option / Quality grade	NN: Option [0099]	
		Q: Grade, A = Automotive, B = Professional	
XX	Product detail	Describes hardware and firmware versions	

Table 22: Part identification code



### 8.3 Ordering codes

Ordering code	Product	Remark	
ZED-F9T-10B	u-blox ZED-F9T		

Table 23: Product ordering codes

Product changes affecting form, fit or function are documented by u-blox. For a list of Product Change Notifications (PCNs) see our website at: https://www.u-blox.com/en/product-resources.



## **Related documents**

- [1] ZED-F9T Integration manual, UBX-21040375
- [2] TIM 2.20 Interface description UBX-21048598
- [3] Product packaging reference guide UBX-14001652
- [4] Radio Resource LCS Protocol (RRLP), (3GPP TS 44.031 version 11.0.0 Release 11)

For regular updates to u-blox documentation and to receive product change notifications please register on our homepage https://www.u-blox.com.

## **Revision history**

Revision	Date	Status / comments
R01	08-Aug-2020	Objective specification
R02	15-Dec-2020	Objective specification Minor text/typo fixes, Alt. limit change to 80km, QZSS sec. updated,USB certification info. added. NMEA ZDA mess. added to default list,AU office No. update.
R03	16-Apr-2021	Advance Information FW ver. TIM2.11
R04	15-Jun-2021	Advance Information FW ver. TIM2.13
R05	28-Jun-2021	Early production information
R06	07-Jan-2022	Early production information FW version TIM2.20; section 1.2: navigation rates updated; section 1.3: NavIC L5 signal enabled; section 4.1: Abs. max. ratings updated; Related docs updated.
R07	18-Apr-2023	Updated I2C and SPI timing specifications in section Communications interfaces
		Updated VCC_RF output current in table Absolute maximum ratings
		Updated backup current in table Operating conditions
		Added timepulse details in table Operating conditions
R08	01-Jun-2023	Updated product status to mass production.
R09	25-Apr-2024	Updated sections:
		Mechanical specifications with information on de-paneling residual tabs
		Qualifications and approvals
		<ul> <li>Information on moisture sensitivity level has been moved from the Integration manual to chapter Qualifications and approvals</li> </ul>



## Contact

#### u-blox AG

Address:
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For further support and contact information, visit us at www.u-blox.com/support.